

PCB
 Markus Koch <markus@notsyncing.net>

Sheet: /
 File: ttl-fpga.sch

Title: DISCRETE TTL FPGA

Size: A4 Date: 2019-05-31
 KiCad E.D.A. kicad 5.1.4

Rev: 02
 Id: 1/3

ISP SPIF

isp_mosiD
isp_sckD
isp_misoD

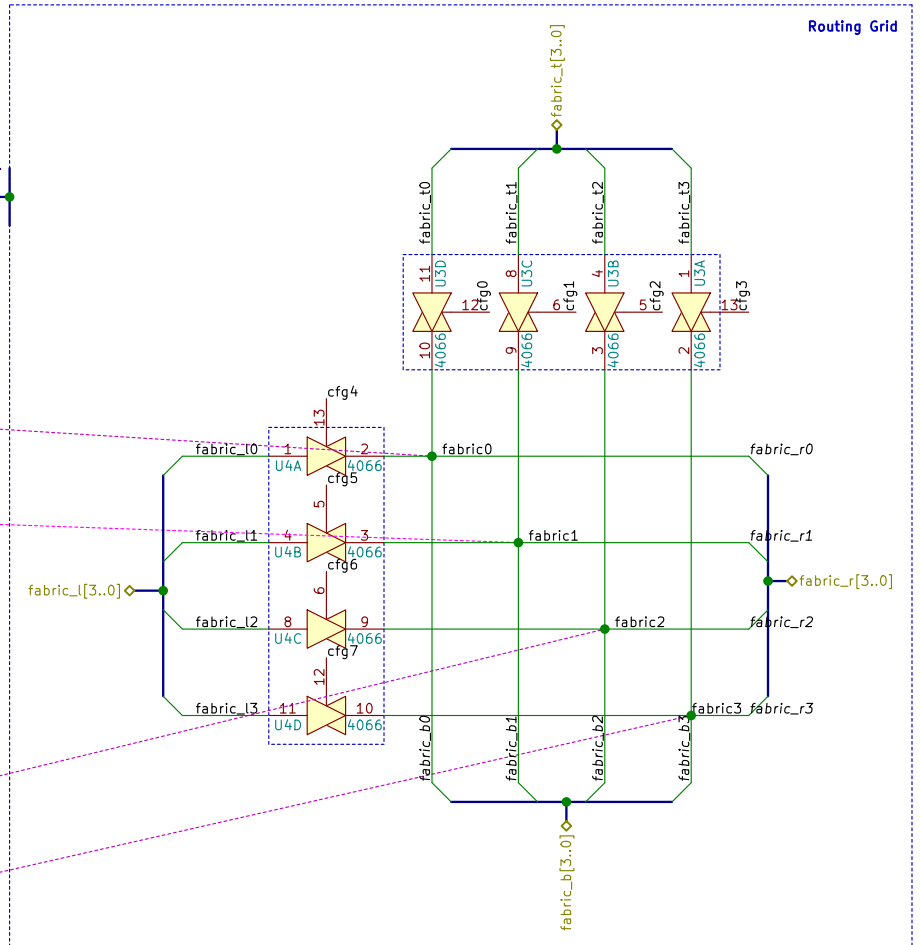
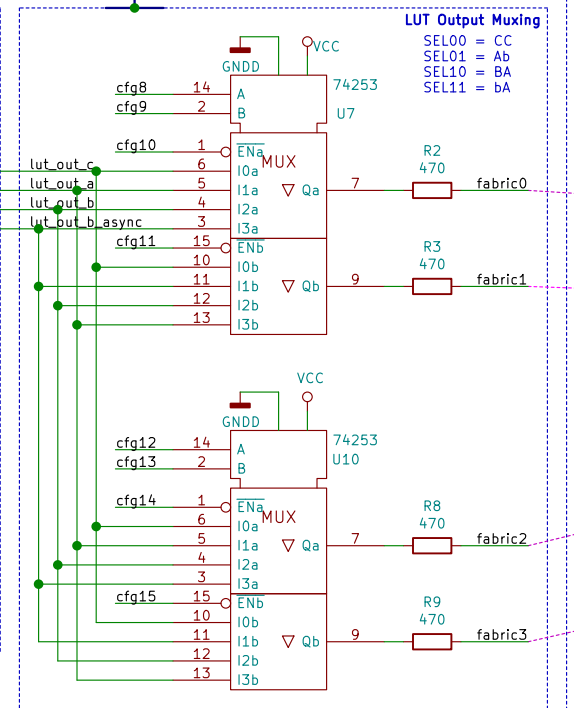
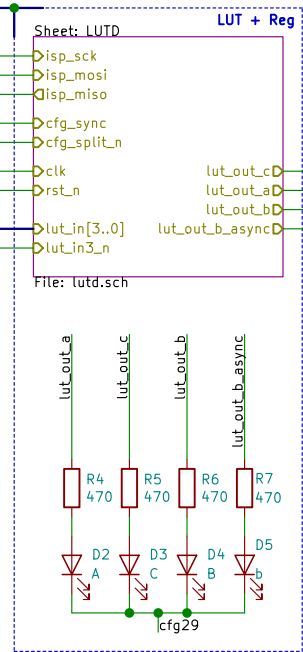
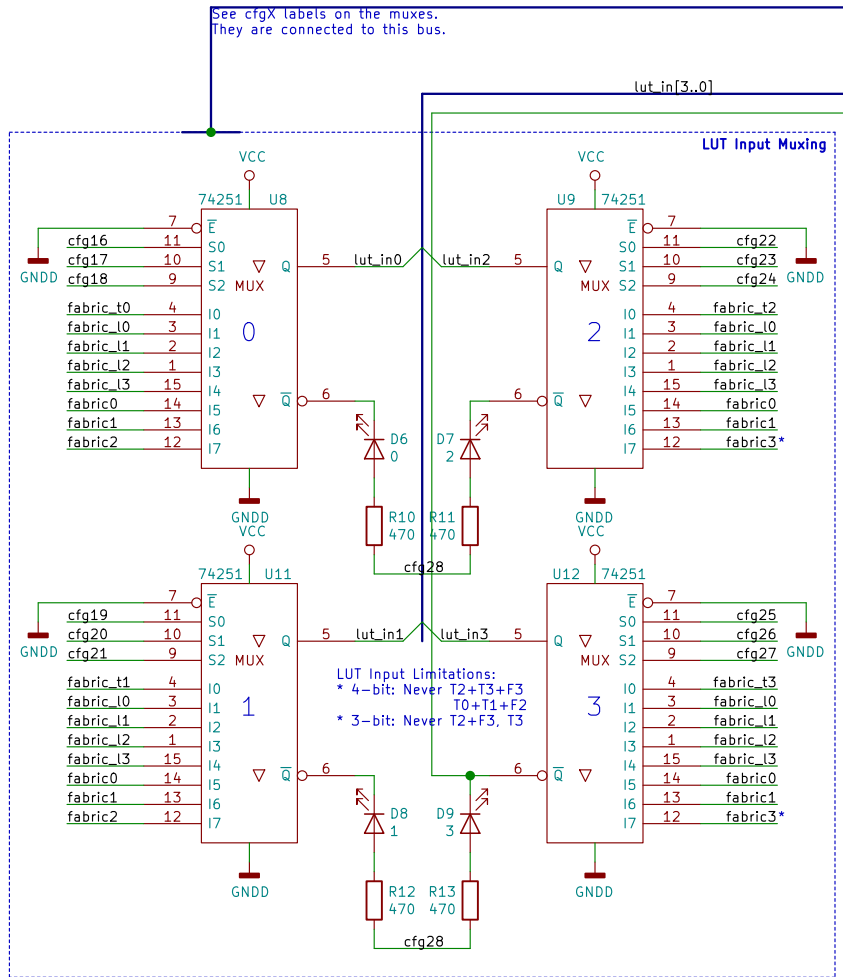
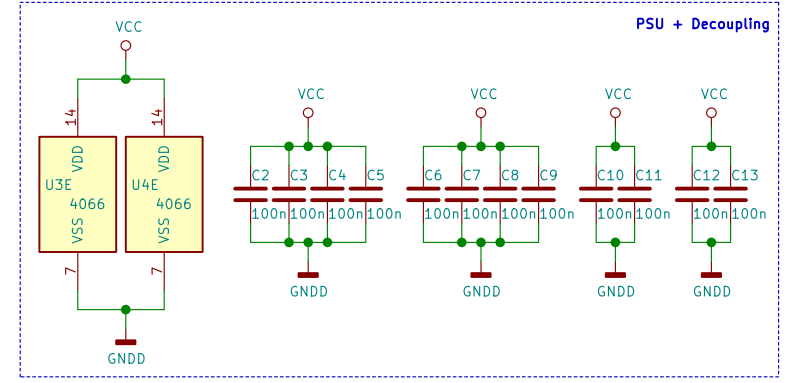
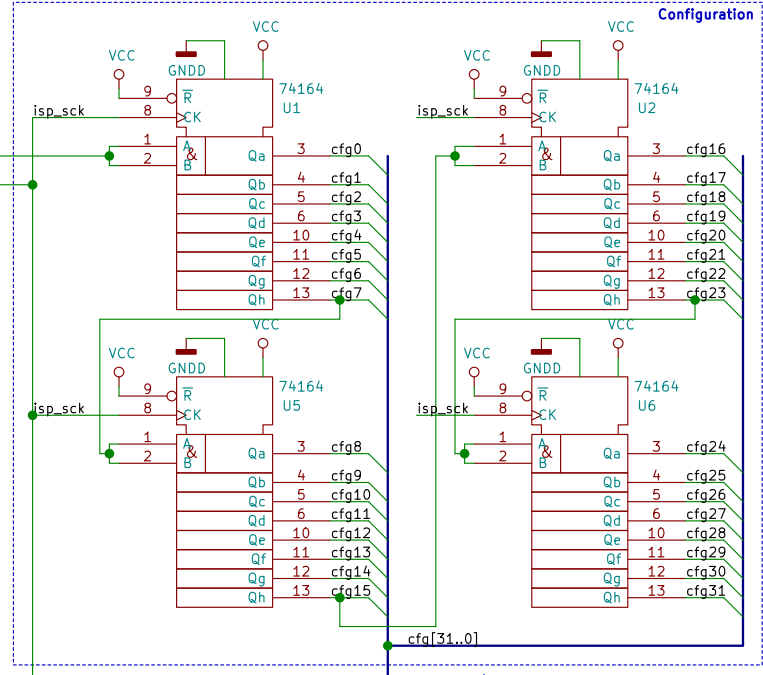
ISP Configuration Bit Mapping:
[3..0]: Route top [3..0]
[7..4]: Route left [3..0]

[9..0]: Output muxing 1&0
[11..10]: Drive 1 / 0
[13..12]: Output muxing 3&2
[15..14]: Drive 3 / 2

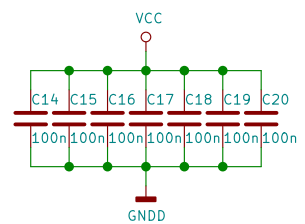
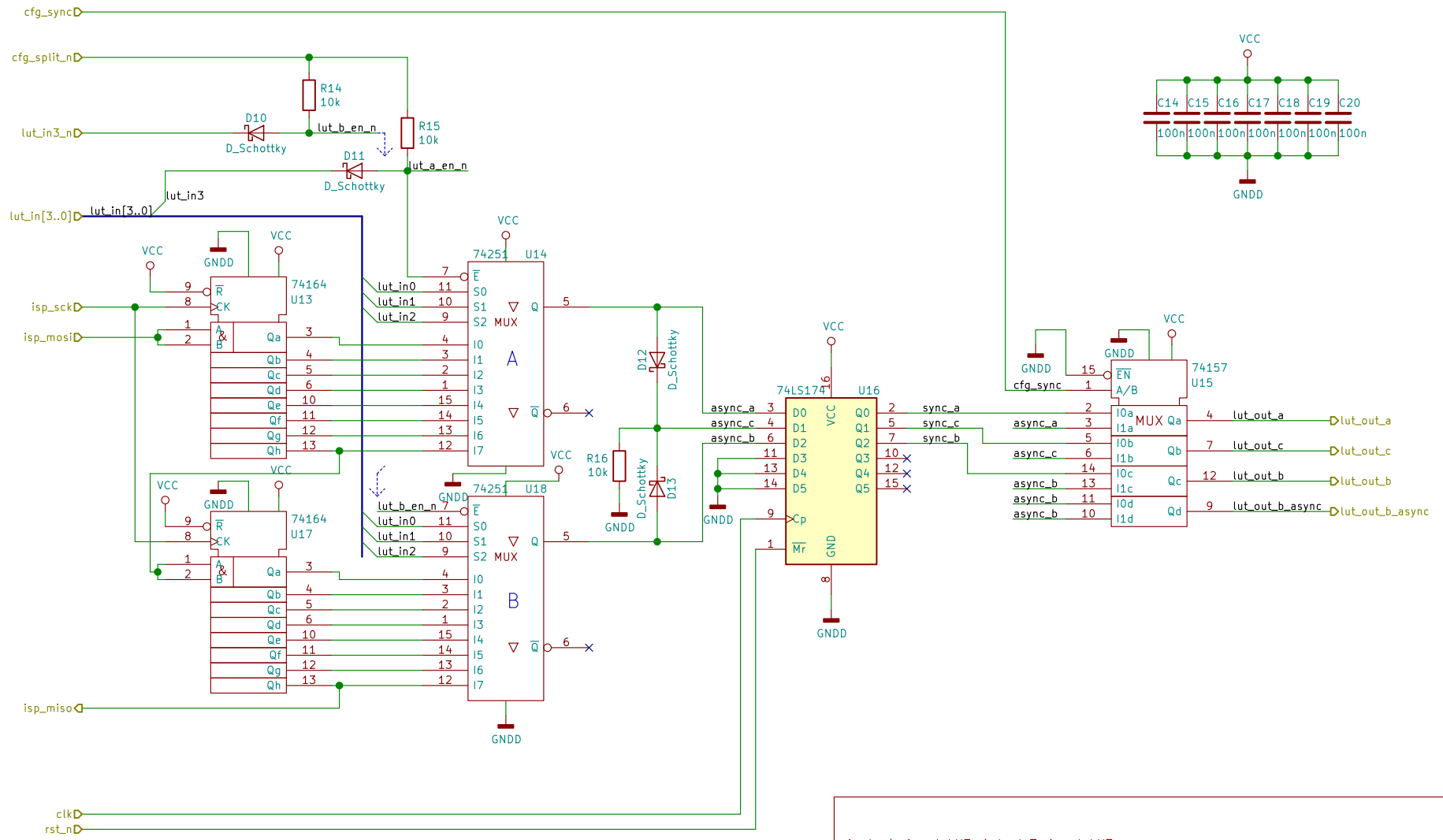
[27..16]: Input muxing
[28]: Input LED enable
[29]: Output LED_enable

[30]: Synchronous mode
[31]: LUT mode _3/4

[47..32]: LUT-4 content
[39..32]: LUT-3/A
[47..40]: LUT-3/B



Logic Block
Markus Koch <markus@notsyncing.net>
 Sheet: /LogicBlock/
 File: logic_block.sch
Title: DISCRETE TTL FPGA
 Size: A3 | Date: 2019-05-31 | Rev: 02
 KiCad E.D.A. kicad 5.1.4 | Id: 2/3



single 4-input LUT / dual 3-input LUT
 Logic Block
Markus Koch <markus@notsyncing.net>
 Sheet: /LogicBlock/LUT/
 File: lutd.sch

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Size: A4	Date: 2019-05-31	Rev: 02
KiCad E.D.A. kicad 5.1.4		Id: 3/3