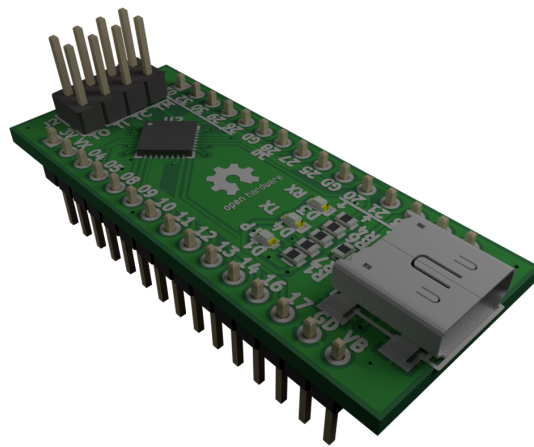


Tiny-X02 Development Kit

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List of Abbreviations

DTR	data terminal ready
FPGA	field-programmable gate array
I/O	input / output
JTAG	Joint Test Action Group
PLL	phase locked loop
LED	light emitting diode
LDO	low-dropout regulator
RX	receive
TX	transmit
UART	universal asynchronous receiver / transmitter
USB	universal serial bus

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1 Introduction

The Tiny-XO2 is a small, versatile and cost-effective development platform for the Lattice MachXO2 field-programmable gate arrays (FPGAs).

In addition to the FPGA, it provides a universal serial bus (USB) to universal asynchronous receiver / transmitter (UART) converter and a crystal to include the basic set of components for any FPGA design.

This manual applies to hardware revision 01. The latest version can be found online at <https://l.entsyncing.net/tinyxo2>

2 Hardware

This chapter explains all available hardware functions.

2.1 Overview

Figure 2.1 and Table 2.1 show an overview of all the functions of the board.

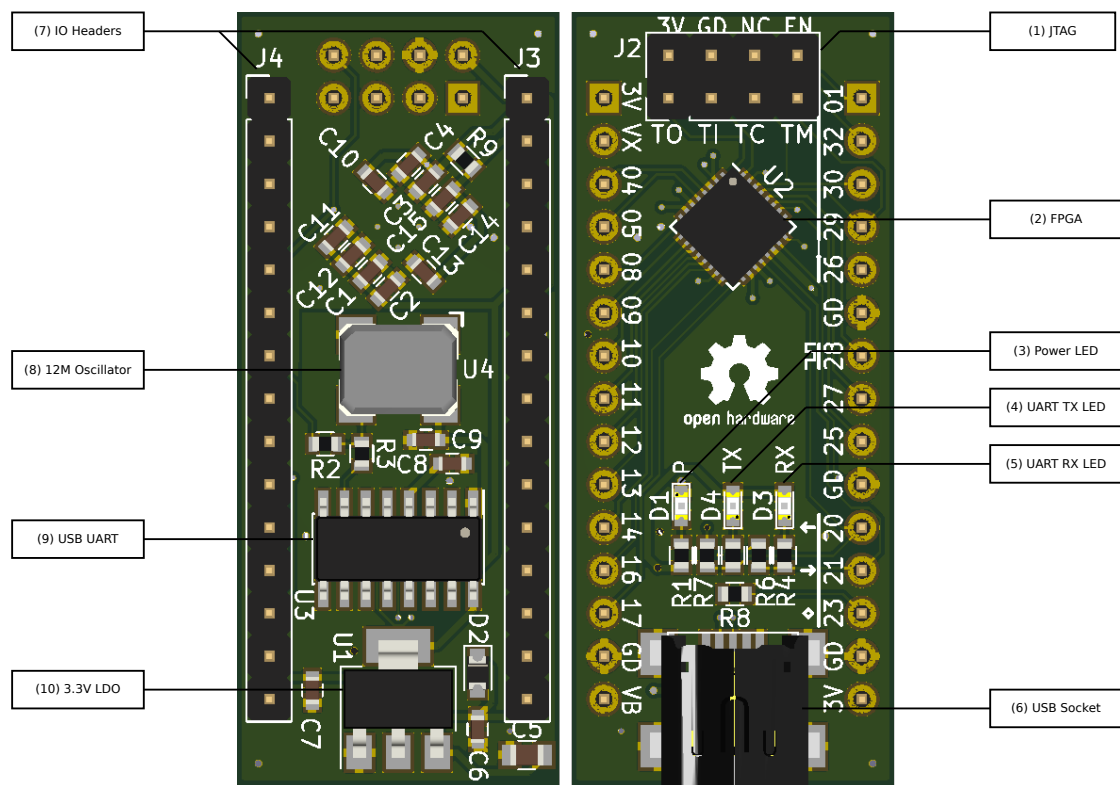


Figure 2.1: Board overview

Table 2.1: Board function list

1	JTAG programming header
2	Lattice LCMXO2-1200HC FPGA
3	Power LED (Orange)
4	UART TX (Board → PC) LED (Red)
5	UART RX (PC → Board) LED (Green)
6	USB socket for UART and power
7	I/O headers
8	12 MHz crystal oscillator for FPGA and USB-to-UART converter
9	CH340G USB to UART converter
10	5 V to 3.3 V low-dropout regulator (LDO)

2.2 Power Supply

The board can be powered either via USB or using the **VB** pin on pin header **J3**. The input voltage can range from 5 V to 15 V [5, page 4]. A diode between the USB jack and the **VB** pin prevents backfeeding of current into the USB connection.

The **3V** pins on the pin headers can be used to supply the on-board generated 3.3 V to supporting circuitry. The maximum current to be drawn from these pins is 500 mA¹.

All input / output (I/O) pins on header **J3** use the voltage on pin **VX** as bank voltage. It may range from 1.2 V to 3.3 V [2, page 8]. By populating **R9** with a zero Ohm resistor, the bank can be connected to the on-board 3.3 V supply. In this case, **VX** becomes a normal **3V** pin.

⚠ Hardware Modification ⚠

If a 2.5 V supply voltage is required for all I/O pins, the main voltage regulator **U1** can be replaced with a 1117-2.5 2.5 V voltage regulator. The FPGA will continue to function normally in this case. When doing this, all **3V** pins carry 2.5 V. **VX** may be supplied with up to 3.3 V. **The CH340G USB-to-serial converter will stop working in this configuration** and needs to be removed from the board.

2.3 FPGA

The FPGA present on the board is a Lattice LCMXO2-1200HC-4SG32C or LCMXO2-1200HC-6SG32C.

¹The maximum current of the AP1117 voltage regulator is 800 mA[5, page 4]. Watch the temperature of **U1** when drawing high amounts of current.

Table 2.2: Main features of the FPGA [3, page 3]

Property	Value
I/O	21*
LUTs	1280
Distributed RAM	10 kbits
EBR SRAM	64 kbits
User flash	64 kbits
Hard IPs	2x I ² C, 1x SPI, 1x Timer / Counter, 1x PLL

** Not all I/Os may be usable, see chapter 2.6.*

Depending on the version of the board, either speedgrade 4 or 6 is installed. Check the marking on the chip to determine which version applies.

2.4 UART and LEDs

The board features a CH340G USB-to-UART converter. Its transmit (TX) line is connected to pin 21, the receive (RX) line is connected to pin 20. Pin 23 is connected to the data terminal ready (DTR) signal from the chip, which is pulled low as soon as the terminal is opened on the PC.

See the markings on the board for a quick reference of the pin functions.

Additionally, the RX and TX lines have an LED connected in parallel. Should a specific LED or UART function be not wanted, refer to table 2.3 to see how to disable individual features.

Table 2.3: Resistors to disable UART functions

Resistor	Description
R6	UART TX
R7	UART RX
R8	UART DTR
R4	TX LED
R5	RX LED

Reset on terminal. By default, the DTR pin is pulled low by the CH340 as soon as the terminal is opened on the PC and remains high while it is closed. This high-to-low transition can be detected using an edge detector inside the FPGA to generate a reset

for the rest of the design.

⚠ Hardware Modification ⚠

If only a short pulse is desired when the terminal is opened, R8 should be exchanged with a 100 nF capacitor and the internal pull-up of the FPGA must be enabled. Now, each time the terminal is opened on the PC, the DTR line on the FPGA will go low for a few ms.

2.5 Crystal Oscillator

The board features a 12 MHz crystal oscillator. It supplies the clock to the USB-to-UART converter and is also connected to pin 28 of the FPGA. If the 12 MHz clock signal is not needed on the FPGA, resistor R2 can be removed to free pin 28 as a general purpose I/O pin. A higher frequency for the design can be generated using the phase locked loop (PLL) inside the FPGA.

⚠ Hardware Modification ⚠

If another base frequency is required, the crystal oscillator on the back (U4) can be exchanged with another value. **The CH340G USB-to-UART coverter will stop working in this configuration** and needs to be removed from the board.

2.6 I/O Headers

The I/O headers break out all available I/O pins of the FPGA. The pin number is marked next to each pin on the board.

Header J3 has no special functions and uses VX as bank voltage. This voltage can be tied to the 3.3 V supply of the board either by installing a zero ohm resistor for component R9 or by installing a jumper between the VX and 3V pin. Refer to chapter 2.2 for more information on I/O voltages.

Header J4 has special functions assigned to most of its pins. Refer to Table 2.4 for a comprehensive list. In order to use these pins as general purpose I/O pins, refer to the respective chapter. All I/O pins on header J4 use 3.3 V as bank voltage.

Note that the Joint Test Action Group (JTAG) pins are connected in parallel to the JTAG header J2 and the corresponding pins on J4.

Table 2.4: I/O pin special functions

Function	Pin	Name	Note
JTAG multiplex	26	$\overline{\text{JTAGENB}}$	See chapter 3.2.2
JTAG	29	TMS	See chapter 3.2.1
	30	TCK	
	32	TDI	
	01	TDO	
UART	20	RX	See chapter 2.4
	21	TX	
	23	DTR	
Clock	28	12 MHz clock	See chapter 2.5

3 Software Configuration

3.1 Comparison

Table 3.1: Comparison of configuration methods

Type	Available I/O	Note
Always-active JTAG	18	Advanced debugging possible
Multiplexed JTAG	21	Special consideration for 4 pins
Bootloader / None	22	Chip can not be recovered on error

3.2 Programming Options

3.2.1 Always-active JTAG

This is the simplest of all configuration methods. It is supported by any Lattice programmer, including the FTDI FTxxxx based ones.

To use this method, no special configuration needs to be applied in the Lattice Diamond software. The programming preferences in the *global preferences* in the spreadsheet view should look like this [1]:

Table 3.2: Preferences for always-active JTAG mode

Name	Value
JTAG_PORT	ENABLE
MUX_CONFIGURATION_PORTS	DISABLE

The following connections need to be made between the programmer and the JTAG header J2: TDO (T0), TDI (T1), TCK (TC), TMS (TM).

Pins 29, 30, 31 and 01 are not available as user I/Os in this configuration. All other pins are available as normal user I/Os.

3.2.2 Multiplexed JTAG

This configuration allows to use the JTAG pins as normal user I/O as long as some parameters are kept in mind.

In this mode, the function of pins 29, 30, 31 and 01 is switched using pin 26 (EN). This pin needs to be pulled low to enable JTAG mode. This can either be done manually before each programming operation or by using the **PROGRAMN** pin available on Lattice programmers. To make the automatic switchover work, the following settings need to be applied in the Diamond software [4]:

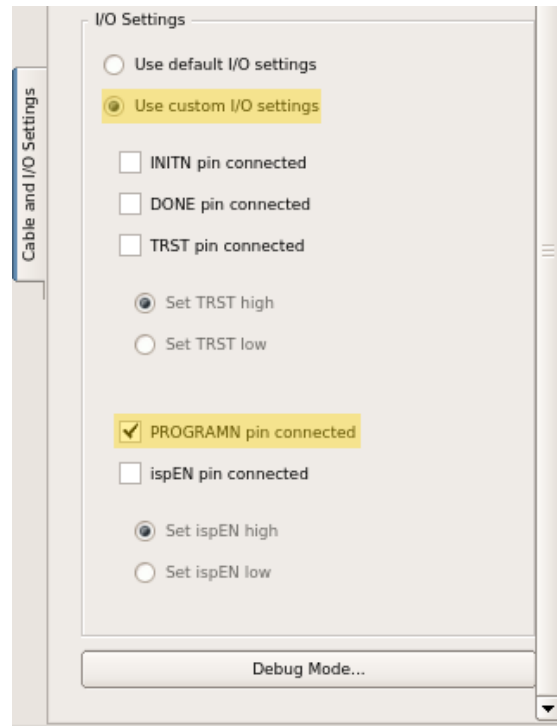


Figure 3.1: JTAG settings for automatic pin multiplexing

To enable this mode, the following settings need to be configured in the *global preferences* in the spreadsheet view in Lattice Diamond:

Table 3.3: Preferences for multiplexed JTAG mode

Name	Value
JTAG_PORT	DISABLE
MUX_CONFIGURATION_PORTS	ENABLE

3 Software Configuration

When programming the FPGA in circuit, the user needs to ensure that all JTAG lines are high-Z during programming (when 26 (EN) is low). Also, the JTAG bit patterns should not affect any components attached to the JTAG pins during a programming operation.

The following connections need to be made between the programmer and the JTAG header J2: TDO (T0), TDI (T1), TCK (TC), TMS (TM), PROGRAMN (EN).

Pin 26 is not available as user I/O in this configuration. Care needs to be taken when selecting which components to connect to pins 29, 30, 31 and 01. All other pins are available as normal user I/Os.

3.2.3 UART Bootloader

The MachXO2 devices can be programmed from the active design. This allows the user to entirely disable all external programming interfaces which makes all I/O pins available to the user logic.

At the current point in time, this functionality has not been implemented.

Warning

Setting these parameters will **permanently** disable the JTAG port. This might render the device unusable. Only apply this if you really know what you are doing.

Table 3.4: Preferences for bootloader mode

Name	Value
JTAG_PORT	DISABLE
MUX_CONFIGURATION_PORTS	DISABLE

All I/O pins are available as user I/Os.

4 Errata

Hardware Revision 01

TLV1117-33 decoupling. The board is missing the 10+ μF capacitor on the output of the 1117-3.3 voltage regulator (U1). This might cause instability with certain devices. This problem can be easily solved by installing a 10 μF 0805 capacitor right next to C7. Revision 02 addresses this issue.

5 Appendix

5.1 Version History

Table 5.1: Version history

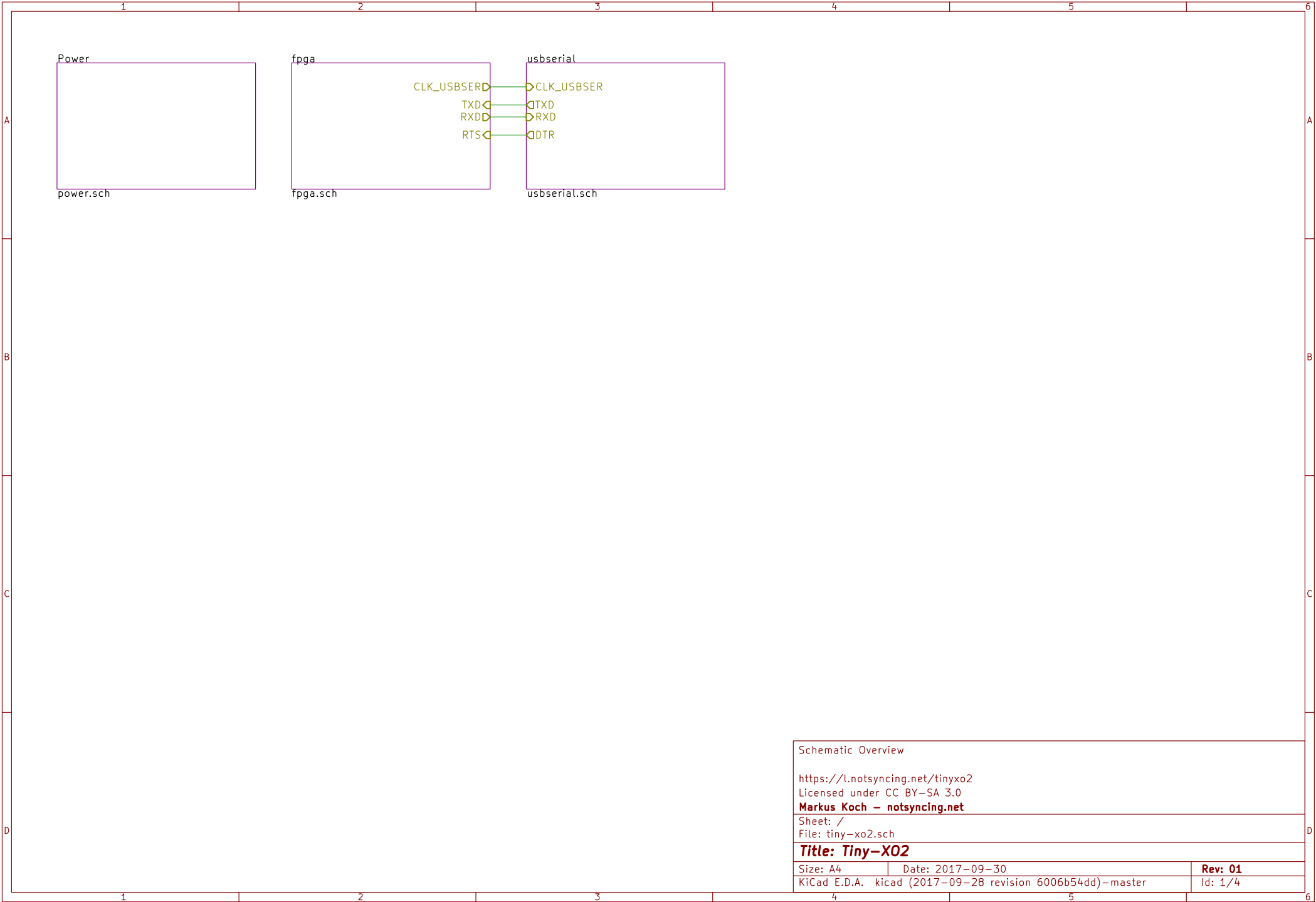
Version	Comment
2017-11-27	DTR usage, 2.5 V mod, errata, editorial changes
2017-11-20	Fix JTAG TDI pin number
2017-11-16	Editorial changes
2017-11-10	Initial draft

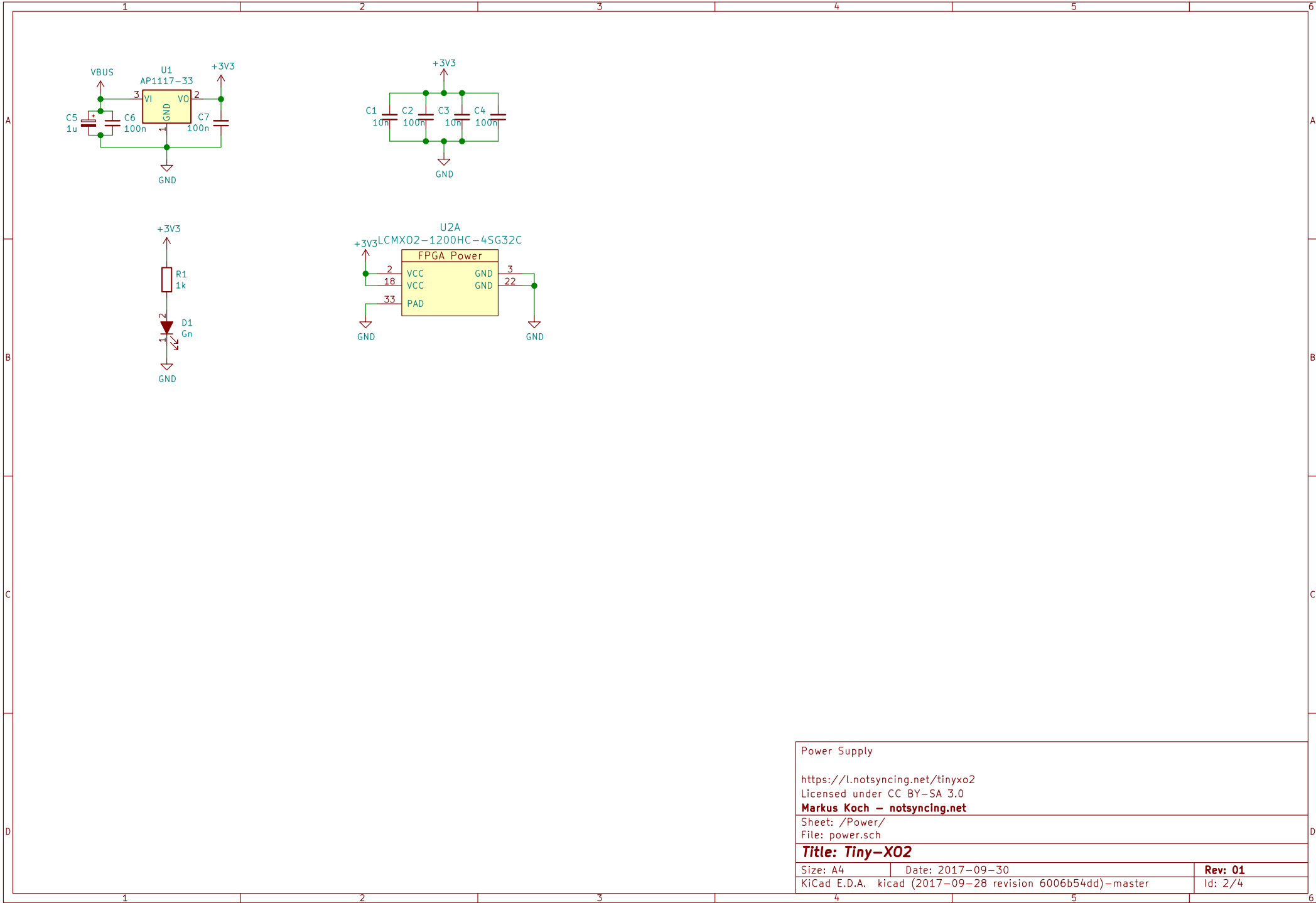
5.2 Bibliography

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- [4] Lattice Semiconductor. *Programming Cables User Guide*. Version 25.0. Nov. 2016. URL: http://www.latticesemi.com/~media/LatticeSemi/Documents/UserManuals/MQ/ProgrammingCableUsersGuide.pdf?document_id=143.
- [5] Texas Instruments. *TLV1117 Adjustable and Fixed Low-Dropout Voltage Regulator*. Dec. 2014. URL: <http://www.ti.com/lit/ds/symlink/tlv1117.pdf>.

5.3 Schematic

See next page.





Power Supply		
https://l.otsyncing.net/tinyx02		
Licensed under CC BY-SA 3.0		
Markus Koch — l.otsyncing.net		
Sheet: /Power/		
File: power.sch		
Title: Tiny-X02		
Size: A4	Date: 2017-09-30	Rev: 01
KiCad E.D.A. kicad (2017-09-28 revision 6006b54dd)-master		Id: 2/4

